REMARKS

Claims 1-50 were pending in the application. By this paper, Applicant has canceled Claims 15 and 33 without prejudice, and amended Claims 1, 7, 13, 16, 23, 26, 28, 32, 45, 46, 47, 48, 49, and 50. Hence, Claims 1-14, 16-32, and 34-50 are presented for examination herein.

Request for Continued Examination (RCE)

Applicant files herewith an RCE for continued prosecution of the above-referenced application.

Title

In response to Par. 4 of the Office Action, Applicant respectfully traverses the Examiner's objection to the Title as amended. Applicant notes that it has previously amended the title in order to address the Examiner's comments. The Examiner has provided no basis for his assertion that the title as previously presented is "not descriptive", and in fact seems to contradict the clear requirement of 37 CFR 1.72 (from MPEP 606):

> *"Title and abstract.*
>
> *(a) The title of the invention may not exceed 500 characters in length and **must be** as short and specific as possible."*

The Examiner selectively cites MPEP 606.01, yet seems to ignore the plain requirements of CFR 1.72. Applicant cannot understand how the title "PROGRAM CONTROLLED EMBEDDED-DRAM-DSP ARCHITECTURE AND METHODS" is considered "non-specific" under the CFR requirements set forth above, or even "non-descriptive" under the passage cited by the Examiner.

Accordingly, Applicant respectfully requests that the Examiner: (i) provide **specific** reasoning or support for his assertion that the title is "not descriptive" or "not specific", and (ii) supply a title which is generic to all claims as presented herein, since Applicant's previous attempts at revision of the title were not suitable to the Examiner.

Requiring Applicant to further include specific attributes or limitations from its claims is an unnecessary restriction on Applicant's right to claim its invention broadly; such additional limitations in the title potentially affecting the claim scope afforded to Applicant.

It is well settled precedent that a patentee is in no way limited to specific embodiments set forth in its specification, and Applicant submits that the inclusion of further aspects of certain embodiments of its invention as requested by the Examiner, that are not generic to all claims, violates the foregoing well-settled principle.

Applicant respectfully submits that the Examiner of record has rejected Applicant's title on clearly improper grounds; i.e., (i) providing no identifiable support or specific basis of his objection, and (ii) clear error in requiring Applicant to include a title which is not generic to all claims.

Objections to the Drawings

Regarding Par. 6 of the Office Action, Applicant traverses the Examiner's assertions and drawing objections set forth in this Paragraph in their entirety. Applicant has read the Examiner's response, yet notes that the Examiner appears to completely ignore Applicant's previous discussion regarding all of the claimed features being present in the drawings as previously presented (See Item (ii) again provided herein below). **The Examiner provides no refutation of Applicant's citations or discussion that each element is already present; he merely in effect says "every element must be shown, and you do not show every element." No basis for why the Examiner disagrees with Applicant's assertion that it already does show every element is provided.**

Furthermore, neither the statute nor the MPEP dictate or in any way require flowcharts as noted by the Examiner. Applicant submits that the Examiner is placing a wholly unreasonable cost burden on the Applicant by in effect forcing the Applicant to generate dozens of flow charts to show every logical flow or feature of every claim.

Applicant therefore submits that the Examiner of record has rejected Applicant's drawings on clearly improper grounds; i.e., clear errors of facts, in that, *inter alia*, all elements of Applicant's claimed inventions are in fact present in the drawings as filed.

Furthermore, Applicant again traverses on grounds that the Examiner is both (i) misinterpreting 37 CFR 1.83 by strictly requiring every element of every claim to be shown in a Figure, including effectively ignoring the several caveats to the general rule set forth in 37 CFR 1.83 and other relevant statutes/guidance; and (ii) ignoring components which are present in the

drawings as filed which perform the precise functions/elements which the Examiner asserts are missing from the claims. Specifically:

(i) 37 C.F.R. § 1.83 states:

> *§ 1.83 Content of drawing.*
> *(a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, **should** be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).*

MPEP 608.02 states:

> *"Any structural detail that is of sufficient importance to be described should be shown in the drawing. (Ex parte Good, 1911 C.D. 43, 164 O.G. 739 (Comm'r Pat. 1911).)"* {Emphasis added}

Applicant notes that: (i) the aforementioned passage of MPEP 608.02 does not say "***must*** be shown", and (ii) the passage qualifies the requirement of illustration in the drawing to those details of sufficient importance. **Under the Examiner's overbroad assertions of Par. 6 of the Office Action, every limitation of every claim must be shown in the drawings (irrespective of its importance), and this position is clearly in contravention of 37 CFR §1.83 and MPEP 608.02.**

Furthermore, the Examiner's logic is flawed when considering hypothetical claims that are comprised of only know or "conventional" elements, yet which are combined in a novel and non-obvious way (and clearly patentable under Supreme Court precedent). Again, the Examiner's interpretation of 37 CFR 1.83 in such a case would yield a result in clear contravention of the aforementioned statutes and rules; i.e., by requiring explicit drawing of elements which are clearly "conventional" and hence not required to be drawn with any specificity per the CFR's and statute.

35 USC §113 states:

> *35 U.S.C. 113 Drawings.*
>
> *The applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented.*

Hence, per the statute, the presence of a drawing of any kind (let alone individual elements thereof) is not required when it is not necessary for the understanding of the subject matter.

Clearly, the Examiner had more than sufficient understanding of all the claimed inventions so as to generate a sixty-one (61) page Office Action, including facially detailed rejections of each claim. Applicant admittedly fails to see how the Examiner can compel the Applicant to submit additional or revised drawings, ostensibly since they are "necessary" under 35 USC §113 and 37 CFR §1.83 for greater understanding, yet clearly have no trouble understanding any portion of the specification or claims during substantive examination.

(ii) Notwithstanding (i) above, Applicant herein traverses the Examiner's assertions that all elements of the claimed inventions cannot be found in the drawings as filed.

For example, Applicant notes the following exemplary passage in the specification regarding "pre-charging" (cited by the Examiner in Par. 6 of the Office Action):

> "*When conditional execution and branching create uncertainties as to what data will be needed, the data and assembly unit may speculatively **precharge** DRAM rows and/or speculatively prefetch data to be used by the functional units 128.*"
> Page 25, lines 12-15, discussing Fig. 1; emphasis added.

Figs. 1 and 2 clearly show the data/assembly unit 122 which performs the pre-charging operation as described above.

Similarly, regarding "deactivation" (also cited by the Examiner as an example of an element missing from the drawings), page 26 of the specification states in discussing Figs. 1, and 2-4:

> *"As will be discussed in greater detail below in connection with FIGS. 2-4, the **data assembly unit 122** is operative to control the DRAM arrays using a set of row-address pointer registers. A set of activation bits is manipulated under program control **to activate or deactivate entire rows of selected DRAM banks** in the DRAM arrays 102, 104, 106."*

Regarding "accessibility" (cited by the Examiner in Par. 6), page 24 of the specification states:

> *"The selector 120 can switch different ones of the register files 112, 114, 116 to be the architectural register file. A selected register file is said to be an active register file. A deselected register file register file is* ***not accessible*** *to the functional units 128 and is said to be an inactive register file."*

Figs. 1 and 2 clearly show all architectural elements necessary to select and deselect register files (including making them "accessible" or "inaccessible").

Regarding the Examiner's citation of the ostensible lack of a drawing showing the "instruction set" (see again Par. 6), Applicant submits that this requirement is (a) nonsensical (i.e., would the Examiner have the Applicant somehow "draw" individual instructions or sets thereof? How does one draw an ephemeral set of electrical impulses, which is what an actual physical implementation of an "instruction" as claimed comprises?); and (b) even if, *arguendo*, the requirement were properly lodged (which Applicant believes it is not), the "instruction set" is a well known and "conventional" feature (see 37 CFR §1.83) which is already illustrated as shown in the form of a "rectangular box" in, *inter alia*, Fig. 1, Reference numeral 124 (instruction cache), Fig. 5, reference numeral 508, and Fig. 6, reference numeral 608 (showing a plurality of exemplary VLIW instructions or "cache lines").

Applicant submits that it has a "rectangular box" for each and every component of its claimed inventions.

Based on the foregoing, Applicant respectfully submits that each of the Examiner's objections of Par. 6 of the Office Action are without merit, and requests that they be withdrawn in their entirety.

Claims Objections

In response to Pars. 7-14 of the Office Action, Applicant has herein amended Claims 7, 13, 16, 28, 32, 45 and 50 to overcome the Examiner's objections of these claims. No new matter has been added.

Claim 15 has been cancelled without prejudice, thereby rendering the Examiner's rejections of this claim moot.

Rejections under §112

Claims 15, 33 and 46-47 are rejected under 35 U.S.C §112, first paragraph, for failure to comply with the written description requirement or failure to comply with the enablement requirement, or both.

By this paper, Applicant has cancelled Claims 15 and 33 without prejudice, thereby rendering these rejections moot. However, Applicant hereby seasonably preserves all rights of traversal of these rejections.

With respect to Claim 46, Applicant has hereby amended Claim 46 to delete the word "parallely", thereby overcoming the Examiner's rejection, since no loading of 2 or more row address registers in parallel (cited as the basis of the Examiner's rejection) is now required by the claim. Accordingly, the Examiner's Section 112 rejection of Claims 46 and 47 is now overcome. However, Applicant hereby seasonably preserves all rights of traversal of this rejection (i.e., that Claim 46 as previously presented fails to comply with the written description requirement).

Per Pars. 20-27 of the Office Action, Claims 15, 26-28, 46-47, and 50 were rejected under Section 112, second paragraph, as being indefinite.

By this paper, Applicant has cancelled Claim 15 without prejudice, thereby rendering this rejection moot.

With respect to Claims 26-28, 46-47, and 50, Applicant has herein amended these claims to overcome the Examiner's rejections. No new matter has been added.

Hence, based on the foregoing, Applicant submits that all of the Examiner's Section 112 rejections have been overcome.

Rejections under 35 U.S.C. §102

Claim 23 –Applicant traverses the Examiner's Section 102 rejection of Claim 23 in that, *inter alia*, there is no teaching or suggestion in Inagami, Paraday (or for that matter Wright) or any combination thereof (including the Examiner's traversed "Official Notice" citation), to provide a processor architecture that includes (i) a row address register that points to DRAM rows, (ii) commands to manipulate the DRAM row address pointer, and (iii) a load command to write an entire DRAM row into a register file.

The Examiner's entire argument for this Claim is predicated on his assertion that "DRAM is very popular" and "it would have been **obvious**...to modify Inagami's main storage to be a DRAM array."

Given the use of the word "obvious" above, Applicant is at a complete loss as to how the Examiner uses this obviousness rejection to bootstrap onto a Section 102 (anticipation) rejection. **For anticipation, each and every element of the claim must be present explicitly or by inherency**. Is the Examiner asserting that DRAM is *inherent* in Inagami? Clearly that would be a fallacious argument.

Furthermore, the Examiner cannot say that, e.g., that Inagami teaches a row address register that points to DRAM rows in the literal sense. Again, under anticipation, this limitation (DRAM) is not in any way taught or inherent in Inagami. The Examiner himself states on page 9 of the Office Action that "*Inagami has not explicitly taught that the memory array is a DRAM array...*".

Hence, Applicant submits that: (i) the Examiner of record has rejected Applicant's Claim 23 on clearly improper grounds; i.e., clear errors of facts; and (ii) the Examiner of record has omitted or failed to provide support for one or more essential elements of each claim currently pending.

Rejections under 35 U.S.C. §103

Claims 1, 6-10, 12-14, 24-25 and 46-48 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Wright.

Claims 2-5, 11, and 26-27 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Parady (5,933,627).

Claims 16-22, 28-45 and 49-50 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Parady, further in view of Bissett (5,896,523).

Applicant notes that Official Notice is taken by the Examiner and used at least once as a basis of rejection for each of the independent Claims above, specifically Claims 1, 13, 16, 23, 28, 45, 46, 48, 49 and 50.

Applicant first traverses all such instances of Official Notice, as discussed below.

1) Traversal of All "Official Notice"

By this paper, Applicant traverses all explicit and implicit "Official Notice" taken by the Examiner in the Office Action per, *inter alia*, MPEP 2144.03C.

(i) **Non-judicious use of Official Notice** - MPEP 2144.03 states in relevant part:

> *"In limited circumstances, it is appropriate for an examiner to take official notice of facts not in the record or to rely on "common knowledge" in making a rejection, however such rejections should be judiciously applied.*
> ...
> *The standard of review applied to findings of fact is the "substantial evidence" standard under the Administrative Procedure Act (APA). See In re Gartside, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000). See also MPEP § 1216.01.*

Applicant further notes that the Examiner is misapplying and stretching the Official Notice he is taking to say it teaches something which it does not. For example, his references shown on, e.g., Page 54, Par. 6 of the Office Action may *arguendo* show that DRAM is greater density, etc. than SRAM, but this is a far cry from the assertions the Examiner is making in his rejections; i.e., **that DRAM is somehow interchangeable with SRAM**. As pointed out in great detail in prior responses and herein, one cannot simply substitute DRAM for the SRAM or other memory types shown in the prior art cited by the Examiner as the primary bases for his rejections. **Significant adaptation and functionality which is not present in the prior art is required to make this substitution**. The Examiner fails to address or dispute this fact. Hence, Applicant respectfully submits that the Examiner of record has rejected Applicant's claims on clearly improper grounds; i.e., clear errors of facts.

Applicant further submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of each claim currently pending; i.e., the functional and structural adaptation to permit use DRAM versus other types of memory.

Further, the Examiner has explicitly utilized "Official Notice" as a basis of rejection in no less than **fourteen (14)** separate instances within the Office Action (**including at least once in each of all ten (10) independent claims presented, thereby causing Official Notice to be a substantive basis of all rejections of all claims, dependent and independent, previously presented**), and further has implicitly used Official Notice in numerous other instances (e.g.,

using the word "inherent" and variations thereof). Applicant submits that this cannot in any way be considered "judicious application" in "limited circumstances" as required by the MPEP.

Applicant notes for example that Official Notice is used twice in each of the rejection of Claim 46. Hardly a judicious use.

(ii) **Improper Use of "Official Notice" as Principal Evidence of Obviousness** – In addition to the foregoing, the Examiner improperly uses such explicit or implicit Official Notice as a critical or principal basis of all of his rejections of the independent claims. Such Official Notice is improper and clearly not in accordance with MPEP 2144.03A&B; *"It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko,* 258 F.3d at 1385, 59 USPQ2d at 1697 {emphasis added}.

Also, as previously noted, the Examiner states the "DRAM and its advantages are well known and expected in the art", and that "DRAM is a very popular memory technology because of ...", but the Examiner provides no basis whatsoever for the proposition that DRAM is interchangeable with SRAM or other memory of the type cited in his primary prior art references; this is because it is not in fact interchangeable with any other type of memory in Applicant's claimed inventions. The Examiner's repeated citation of Official Notice throughout the Action for the foregoing propositions comprises an improper use of Official Notice pursuant to MPEP 2144.03 A-C. Applicant's invention of, e.g., Claim 1 utilizes a specific optimized architecture including an embedded DRAM processor that interfaces directly to DRAM.

The Examiner's use of Official Notice in this instance is akin to asserting that a hypothetical claimed monoplane (single wing aircraft) is obvious over (i) bi-plane prior art, combined with (ii) Official Notice that "use of a wing" is well known. Clearly, the invention of the monoplane required additional inventive novelty and inventive step over the bi-plane prior art. The entire architecture of the claimed monoplane (e.g., wings, fuselage, landing gear, etc.) is adapted specifically for a craft with a **single** set of wings. Hence, the Official Notice of "a wing" is improperly used as the primary basis of the rejection, being "boot-strapped" to the bi-plane art to ostensibly teach or suggest something which it clearly does not (i.e., an aircraft with a single set of wings capable of flying).

Applicant also notes that *"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103."* In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; *"The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art."* **None of the art cited by the Examiner recognizes the problem Applicant's inventions seek to address. In the context of Applicant's analogy, none of the "bi-plane" art ever recognizes the need for a single set of wings, or conversely the problems with two or more sets of wings.**

Per MPEP 2144.03C, Applicant hereby requests that the Examiner provide explicit references that teach an embedded DRAM processor with the functionality of the claimed inventions, since the Examiner has failed to do so to this point. None of the cited art including Inagami, Wright, Parady, Hennessy, etc. teach or even remotely suggest an embedded DRAM processor, as set forth in Applicant's claims. What the Examiner has done to date is show art for: (a) a processor, and (b) DRAM; this does not in any way equate to an *embedded DRAM processor*.

Furthermore, Applicant notes that in response to the Examiner's comments on page 54, par. 86 b), Applicant has herein amended every independent Claim to include limitations in the body of the claim and the preamble regarding the recited DRAM array and processor being "embedded". The Examiner now must afford these limitations patentable weight. Applicant therefore again reiterates its call for the Examiner to provide tangible prior art that shows an embedded DRAM processor.

Per MPEP 2144.03C, Applicant also hereby requests that the Examiner provide explicit references that teach register "move" functionality in the context of an embedded DRAM processor, since the Examiner has failed to do so to this point.

(iii) **Improper Use of Official Notice on Final Rejection** – Applicant respectfully directs the Examiner's attention to MPEP 2144.03, which states:

> *While "official notice" may be relied on, these circumstances **should be rare** when an application is under **final rejection** or action under 37 CFR 1.113.* {Emphasis added}

Applicant notes that per the Office Action, the current application is presently under final rejection. Applicant submits that the use of fourteen (14) separate explicit instances of Official Notice (without even counting those of an implicit nature), with some claims being rejected based on two separate notices, cannot in any way be considered "rare". **Every independent claim finally rejected by the Examiner in the Office Action finds its basis of rejection in Official Notice.**

Applicant notes that the aforementioned passage of MPEP 2144.03 places yet additional burden and restrictions on the Examiner over those of "judicious" use in "limited circumstances" as set forth in Item (i) above, based on the final-rejection status of the Application.

(iv) **Each Instance of Official Notice is Unique** – In addition to the foregoing, Applicant traverses the Examiner's statements on page 54 of the Office Action regarding only his use of Official Notice essentially only "5 times". Each claim is a different invention, and hence the use of Official Notice in each instance is unique, since each Claim is unique. The Examiner focuses on the numerology, but instead should focus on the fact that every independent Claim presented by Applicant is rejected based on Official Notice. In the present context, Applicant's issue with the Examiner's application of Official Notice is *not* the number of times it is used *per se*, but rather the number of times it is used as a basis of rejecting highly varying and different inventions (claims). The Examiner respectfully uses the same Official Notice, in fact verbatim in many cases, to fill in any holes remaining in his arguments which he cannot otherwise fill via prior art, without examining or considering the specific application of that Official Notice in each specific claim (invention). With all due respect, everything appears obvious to the Examiner, since he can always cite Official Notice to fill in any such holes left by the prior art, irrespective of whether use of Official Notice in each different context is correctly applied. Such "blanket" usage of Official Notice is improper.

Based on items (i)-(iv) above, Applicant submits that the Examiner has improperly utilized all instances of Official Notice in rejecting, *inter alia*, Claims 1, 13, 16, 23, 28, 45, 46,

48, 49 and 50, and that all such rejections predicated on "Official Notice" (whether explicit or implicit) must be withdrawn.

2) Substantive Section 103 Rejections

a) Claims 1, 6-10, 12-14, 24-25 and 46-48 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Wright.

Claims 1, 13, 46 and 48 - Inagami, it was asserted, teaches most of the claimed elements of Claim1 except the use of DRAM and the DRAM associated operation such as precharging and deactivating. Applicant traverses.

Claim 1 describes a system that enables precharging. The row register address register of the claimed invention is wholly different from the vector address register 60 of Inagami because the row register address register of the present invention can be used (for example, as an operand in DRAM row-based applications) in precharge-row and deactivate-row instructions. For example, one possible use of this functionality (although by no means an exclusive or only use) is to speculatively precharge a row before it is actually used. The row can be speculatively precharged in advance of one or more load/store operations. Subsequently, a long string or a shorter burst of load store operations can be performed without the need to keep recharging the row. This improves the effective bandwidth of the DRAM. After the program no longer needs to access the row, the deactive instruction can be given and another row can be precharged. When multiple banks of DRAM are available, the data assembly unit can precharge different rows in different banks of DRAM. **Neither Inagami, nor any of the other cited art, teach or suggest such pre-charging functionality in any way.**

Hence, Applicant submits that the Examiner of record has rejected Applicant's Claim 1 on improper or erroneous grounds by omitting or failing to provide support for one or more essential elements of Claim 1.

Additionally, the SDRAM commands in Wright are hardware layer memory commands sent directly to the DRAM device, and hence Wright does not teach or suggest the use of the use of a row address register nor a precharge command nor a deactivate command as taught by Applicant. Applicant reminds the Examiner of the plain language of Claims 1 (and similar language in Claim 13):

*an **instruction set** which includes:*

(i) ...

(ii) a command to precharge (activate) the row pointed to by said row address register;

(iii) a command to deactivate said row pointed to by said row address register after it had been precharged by the command to precharge;... {Emphasis added}

Applicant similarly traverses the Examiner's inherency argument on, *inter alia*, page 12; i.e., that the "command" is deemed inherent because rows will stay activated if not deactivated. **There is simply no command (i.e., part of an instruction set) taught by Wright. How is a code or software instruction inherent in a hardware DRAM?**

Applicant therefore respectfully submits that in addition to the prior errors: (i) the Examiner of record has rejected Applicant's Claims 1 and 13 on clearly improper grounds; i.e., clear errors of facts on what is "inherent" in a reference; and (ii) the Examiner of record has omitted or failed to provide support for one or more essential elements of each of Claims 1 and 13.

Applicable portions of the foregoing distinctions are relevant to Claims 46 and 48 as well.

Furthermore, Claims 46 and 48 include limitations relating to the recited loading of selected columns of rows pointed to by the recited row address registers into designated sets of said data registers being performed in response to an instruction issued **after** the precharging. Inagami '168 in no way teaches or suggests load/store operations that are in response to an instruction issued after precharge.

In fact, under the Examiner's assertions of "Official Notice" relating to DRAM, the load/store instruction itself would comprise the "precharge" instruction, and hence Inagami combined with the Examiner's Official Notice clearly *teaches away* from Claims 46 and 48 as presented herein.

Applicant therefore respectfully submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of each of Claims 46 and 48.

Applicant therefore submits that independent Claims 1, 13, 46 and 48, and all other claims that depend therefrom, are in condition for allowance.

b) Claims 2-5, 11, and 26-27 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Parady (5,933,627). Applicant respectfully traverses these rejections in their entirety.

Claims 2-5 - Regarding Claim 2, the Examiner asserts that Paraday teaches that a command to select of a first and second sets of registers to be an architectural set of registers accessible to said first set of functional units. In particular, the Examiner asserts this element is disclosed by components 38 and 40 of Fig 1 which are found to comprise functional units that may be coupled to register files 50 along with the description set forth in Col. 1, lines 18 – 39.

Applicant disagrees with examiners characterization of the Paraday reference. In particular, Paraday teaches the use of threads which are assigned sets of registers in which to perform the associated processing tasks. However, the threads do not correspond to any particular function element such as component 38 or 40 or Fig 1. The threads are simply different sets of software executed in round robin fashion. Thus any component in Fig.1 could by used by any thread at a given time. Thus, Examiner has mischaracterized Paraday in that Paraday does not teach the claimed element.

In light of this, Applicant submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of Claim 2.

Furthermore, the Examiner has failed to cite any motivation or suggestion to combine Paraday and Inagami references. Without such a suggestion or motivation for combination the use of these two references together to anticipate the claimed subject matter is improper.

Applicant further argues that any combination of Paraday and Inagami would be inoperable and therefore is improper. One can, to overcome an obviousness rejection, show that "the claimed combination cannot change the principle of operation of the primary reference or render the reference inoperable for its intended purpose." *See* MPEP § 2143.01. In particular, Parady attempts to achieve additional processing power by performing vector processing of mathematical operations. Vector processing requires the highly controlled manipulation of the data being processed to ensure that is available in the correct order at the correct time at the various processing units.

Paraday, in contrast, seeks to achieve additional processing power by performing threading on a single micro processing unit. In this case the threads are completely independent, and no special configuration of the data is required. Any attempt to combine Paraday with Inagami would be inoperable as the use of completely independent threads of Paraday would make the vector processing of Inagami impossible. The threads lack the organization and structure necessary for any sort of vector process.

Similarly, the requirement of highly organized data of Inagami would eliminate the benefit provide by Paraday of providing some degree of parallelism using conventional software tools and programs. Thus, any combination of Paraday on Inagami would be non-operable and change the principle of operation of Inagami, therefore such combination is improper.

In light of this, Applicant submits that the Examiner of record has erroneous relied on a clear error of fact; i.e., that the two references can be combined at all.

For similar reasons, as well as the additional limitations set forth therein, Applicant submits that Claims 3-5 also set forth allowable subject matter.

Claims 11 and 26-27 - Regarding Claims 11 and 26-27, the Examiner has failed to cite any motivation or suggestion to combine Paraday and Inagami references. Without such a suggestion or motivation for combination the use of these two references together to anticipate the claimed subject matter is improper. Applicant submits that there would be no motivation to combine Paraday with Inagami because the vector processor does not need to do thread switching, and also the thread switching has nothing to do with the claimed invention. The claimed invention uses the active/inactive registers to implement an efficient DRAM interface to keep a single thread busy. While the current invention could work in a multithreaded environment, the claimed invention is performing an intelligent caching function.

In light of this, Applicant submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of Claims 11, 26 and 27.

c) Claims 16-22, 28-45 and 49-50 are rejected under 35 U.S.C. §103 as being unpatentable over Inagami in view of Parady, further in view of Bissett (5,896,523). Applicant traverses each of these rejections.

Specifically, Inagami teaches away from the use of DRAM and that Inagami fails to teach or suggest how to combine its disclosure with the use of DRAM as the interface and functionality of DRAM is substantially different than the memory of Inagami. In light of this, Applicant submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of independent Claims 16, 28, 49 and 50.

Furthermore, Applicant submits that any combination of Paraday and Inagami would be non-functional as both attempt to solve similar problems (processing different data stream) in completely different and incompatible ways. As previously noted, one can overcome an obviousness rejection by showing that "the claimed combination cannot change the principle of operation of the primary reference or render the reference inoperable for its intended purpose." *See* MPEP § 2143.01. **At absolute minimum, one of the aforementioned references would have to change its principle of operation to make Applicant's claimed invention(s).**

Applicant also notes that *"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103."* In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; *"The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art."* **None of the art cited by the Examiner recognizes the problem Applicant's inventions seek to address**. Applicant requests that the Examiner re-read the "Background of the Invention" Section of Applicant's specification as filed to gain an appreciation for what problems Applicant sought to overcome with its invention; these are clearly not recognized by any of the prior art, whether alone or in combination.

In light of these multitude of different bases of error, Applicant further submits that the Examiner of record has relied on a clear error of fact; i.e., that the two references can even be combined to produce Applicant's claimed invention(s).

In addition to the arguments recited above, Applicant further notes that the general description of performing data prefetches in the background Examiner cites is Bissett is merely a

generalization and in no way teaches or suggests all of the corresponding elements set forth in Claim 16. In particular, Claim 16 sets forth:

> *"...a command to load a set of selected elements of the row pointed to by said row address register into a selected set of said data registers, said selection based on bits in said bit mask, and the selected set of said data registers being in the inactive state...."*

These limitations of Claim 16 set forth far more than just the general concept of performing a data prefetch as disclosed in Bissett. They include (i) a command to load a set of selected elements of a row pointed to by a row address, and (ii) that the selected set of data registers is inactive, and determined by a bit mask. This is far more than just a general prefetching operation.

Given Bissett's failure to disclose all of these claimed elements, Applicant submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of Claim 16.

Applicant provides similar arguments for applicable features of independent Claims 28, 45, 49 and 50.

Other Remarks

Applicant hereby specifically reserves all rights of appeal, including those under the Pre-Appeal Brief Pilot Program, as well as the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned Action, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such claim cancellations or additions.

Furthermore, any remarks made with respect to a particular claim or claims shall be limited to only such claim or claims.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

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